The disclosure has been objected to for informalities enumerated in the Office action.

Accordingly, the specification has been corrected by amendment to obviate the objection.

Claims 1-4 stand rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,117,377 to

Finman (hereinafter "Finman") in view of "Pattern-Independent Current Estimation for

Reliability Analysis of CMOS Circuits" by Burch et al. (hereinafter "Burch"). Claims 5-8 stand

rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,784,285 to Tamaki et al. (hereinafter

"Tamaki") in view of Burch. Claims 1-8 are amended herein and, for the following reasons, are

now patentable over the prior art of record.

Applicant's undersigned representative would like to thank the Examiner for granting the

telephone interview conducted on April 6, 2004. As discussed in the interview, prior art

references Finman (U.S. Patent No. 5,117,377) and Tamaki (U.S. Patent No. 5,784,285) teach

using measuring current flowing through actual nodes of actual circuits, and using this measured

data to perform their calculations. In contrast, the instant application discloses using a simulation

of a circuit to estimate current waveforms at simulated nodes. The Examiner agreed that the

cited prior art does not teach a simulation as in the instant application. Therefore, as discussed

with the Examiner, claims 1 and 5 has been amended to more clearly distinguish the present

invention from the prior art by inserting the word "simulated" in their respective preambles, and

claims 1-8 have been amended to insert the word "simulated" before each occurrence of the word

"node." Thus, since every limitation of the claims in not taught or fairly suggested by the

references, claims 1-8 are now patentable over the prior art of record.

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If there are any additional fees resulting from this communication, please charge the same to our Deposit Account No. 16-0820, our Order No. 32809.

Respectfully submitted,

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April 12, 2004